



Application Note

AN_386

FT600 Maximize Performance

Version 1.0

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Data transfer through USB devices depends on many factors. This application note discusses how to optimize throughput by making use of FT600 and FT601 FIFO buffer.

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1 FTDI FT600 and FT601 USB 3.0 to FIFO Bridge

FT600 and FT601 are FTDI USB 3.0 to FIFO interface bridge chips. The chips handle USB 3.0 protocol and transfer by themselves. The chips provide flexible configuration on the parallel interface, offering either single or multi-channel FIFO interfaces.

When designing with the FT600 and FT601, the user can focus on the data transfer between simple parallel interface rather than the USB 3.0 protocol. This greatly reduces the development time and effort.

2 FT600 and FT601 FIFO interface

FTDI FT600 and FT601 provide 2 types of parallel FIFO interface, 600 and 245 modes. The 245 interface mode is similar to that which can be found on the FTDI FT232R and FT232H serial products. To cater for the higher data rate, FT600 and FT601 are synchronous parallel bus designs. FT600 and FT601 provide a 100 MHz reference clock to the FIFO master, the data word is presented at the FIFO interface back to back at 100 MHz clock in the FIFO bus transactions.

FTDI USB 3.0 bridge chips come with 2 chip packages targeted for different user requirements. The FT601 is designed for higher throughput with a 32 bit parallel data interface, the max FIFO throughput is 400 Mbytes/s. The FT600 is a design for small pin count with 16 bit parallel data interface, the max FIFO throughput is 200 Mbytes/s.

2.1 FTDI USB3.0 FIFO bridge throughput

Although the USB 3.0 specification has a line speed of 5 Gbps, in reality, the overall data transfer rate is the result of the combination on the performance of the PC hardware, the OS, the USB XHCI host, the USB host driver, the USB device driver, the application and the USB 3.0 device design.

In this document, we will not address the theoretical max data rate USB 3.0 can reach, but rather, we will take the FT601 data transfer demonstration as an example to illustrate the effective data throughput between the USB application and the FIFO master design, which is much more closer to the real implementation that users will do with the FT601.

In this document, we assume that the PC speed, the OS, the USB XHCI host and the XHCI host driver are well performing and the USB speed is 5 Gbps, above the FIFO interface at 3.2 Gbps max (400 Mbytes/s for FT601), we will evaluate performance contribution of the application, the USB device driver and FIFO master interface design. A dedicated section below describes design consideration of the FIFO master to improve the system throughput.

2.1.1 The performance of the application and the USB device driver

FTDI delivers the D3XX driver for the FT600 and FT601 USB devices. The device driver is designed to handle the high data throughput, it supports the asynchronous overlapped the USB data transfer. This means the user's application can issue multiple data transfers to the D3XX driver. With this design, the gap between the data transfers are minimized and so data rate for a continuous data stream is improved.

The D3XX driver and FT600 design support continuous streaming data transfer. The application can setup the FT600 channels for one time, the USB data IN and OUT channels will be open for data streaming until a stop command is issued.

2.2 FT601 data transfer performance demonstration setup

2.2.1 Data transfer environment setup

The performance demonstration is based on FTDI data streaming application and a data source/sink FPGA design.

Windows version: Windows 7 SP1 x32, Lenovo ThinkCentre Edge, Intel® Core i7-3770, 3.4 GHz, 8 GB Memory.

Application: FTDI data streamer, driver D3xx version 1.0.0.5.

Hardware: UMFT601X module, Xilinx® Spartan-6 FPGA SP601 evaluation kit.

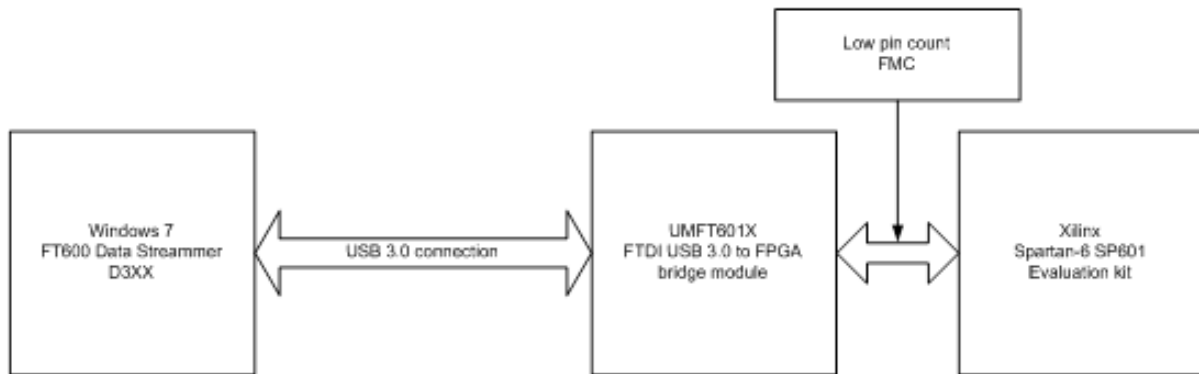


Figure 1 performance demo setup diagram

In this demonstration, the FPGA is designed so that it will read data from the OUT FIFO channel, whenever it is ready, and fill up the IN FIFO channel whenever it is empty.

The FTDI data streamer application will send out data to FT601 or read in data from FT601 once the test starts.

2.2.2 FT600 and FT601 internal FIFO size and configuration

The FT600 and FT601 FIFO mode and the FIFO size configuration are listed in below.

Mode	Channel number	FIFO size for each channel (double buffered)
245	1 in and 1 out	4 KB
FT600	1 in and 1 out	4 KB
FT600	2 in and 2 out	2 KB
FT600	4 in and 4 out	1 KB
245 IN only	1 in	8 KB
245 OUT only	1 out	8 KB
FT600 IN only	1 in	8 KB
FT600 OUT only	1 out	8 KB

Table 1 FT600/FT601 mode configuration and FIFO size for each channel

In a high data rate application design, most of the time; the application will initiate a transfer which consists of multiple of USB packets. In this case, the FIFO master normally can read or fill up the FIFO in full FIFO size in one bus transactions. It happens that at the end of USB transfer, there will be a short packet that indicates the end of the current transfer.

To handle this scenario, the FT601 and FT600 design monitors the FIFO interface transaction, once the FIFO transaction stops, even before the FIFO is full or empty, the FT601 and FT600 will consider the data ready to process, and complete the current USB transfers.

For example, if the FT601 is configured in 1 channel, IN FIFO size is 4 KB, if the FIFO master writes 3 KB data to the IN FIFO and stops, the FT601 will get control of the current FIFO and

forward the data to USB interface. In the meantime, the FT601 will provide the next available FIFO to the FIFO master to fill up more data.

For the USB out transfer, it is recommended that the FIFO master should read out all the available data in the FIFO in one FIFO bus transaction.

2.2.3 FIFO interface timing diagram

In the below example the FIFO interface timing diagram is used for FIFO bus efficiency analysis.

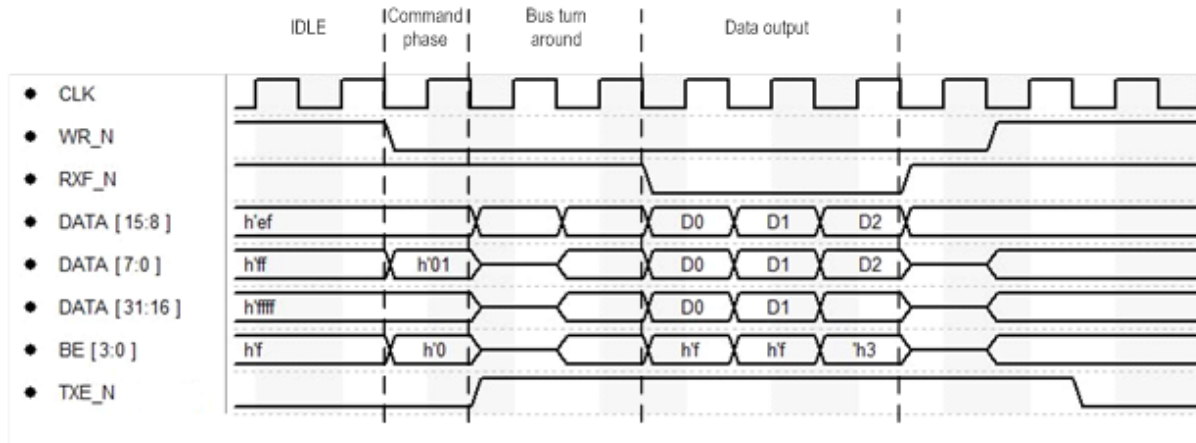


Figure 2 FT601 FIFO timing diagram

FIFO read (USB out transfer) efficiency calculation:

$$= \text{Data output} / (\text{IDLE} + \text{Command Phase} + \text{Bus Turn Around} + \text{Data output})$$

For example, if idle cycle is 150 and the FT601 configuration is 1 channel, FIFO depth is 4 KB, then the FIFO read efficiency is $(4096/4 \text{ (word at FIFO interface)}) / (2+1+1+4096/4) = 87\%$

and below give the calculation of FIFO bus data rate when the IDLE time and FT601 FIFO depth vary.

Note:

1. The idle cycles can either come from the FIFO master when handles the FIFO switching, the FT601 internal configuration and also the USB host transfer speed.
2. In multi-channel FIFO mode, the USB host operates individual channels access fairly so that the FIFO master can read or write one channel to another channel with less IDLE cycles. The combined data rate of multiple channels will be higher than the demonstration at single channel only. It also depends on the system performance.

	Idle	CMD	TURN	FIFO depth	Efficiency	Data rate (MB/s)	Idle	Efficiency	Data rate (MB/s)
1	150	1	2	1024	62.59%	250.37	200	55.77%	223.09
2	150	1	2	2048	76.99%	307.97	200	71.61%	286.43
3	150	1	2	4096	87.00%	348.00	200	83.46%	333.82
4	150	1	2	8192	93.05%	372.19	200	90.98%	363.93

Table 2 FIFO efficiency

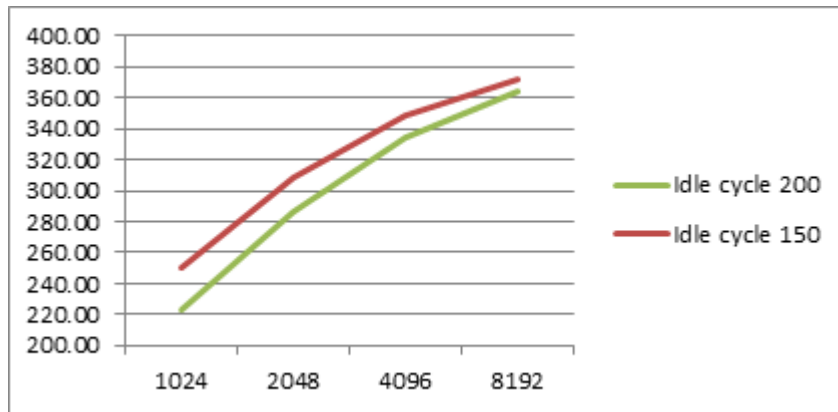


Figure 3 FIFO throughput vs FIFO size

Table 3 and Figure 4 below gives FIFO data rate when the idle period changes.

	Idle	CMD	TURN	Efficiency	Data rate (MB/s)
1	120	1	2	4096	89.28%
2	140	1	2	4096	87.75%
3	160	1	2	4096	86.27%
4	180	1	2	4096	84.84%
5	200	1	2	4096	83.46%
6	220	1	2	4096	82.12%
7	240	1	2	4096	80.82%
8	260	1	2	4096	79.56%
9	280	1	2	4096	78.35%
10	300	1	2	4096	77.17%
11	320	1	2	4096	76.02%

Table 3 FIFO data rate vs idle cycles in one channel mode (FIFO size is 4 KB)

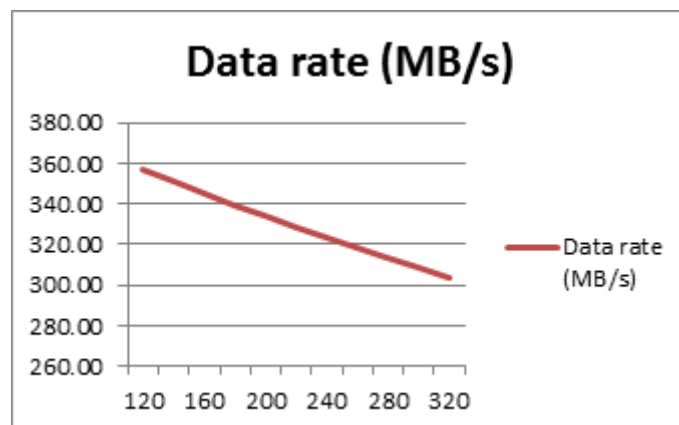


Figure 4 FIFO data rate vs idle cycles for one channel

2.2.4 Optimize the application and FIFO master design to get the max data rate

From the tables and figures in section 2.2.4, we can observe that if the FIFO master wants to get the max data throughput, the design should consider having a bigger FIFO size and also reduce the idle cycles between FIFO bus data transactions.

There are other things the application needs to take into account, as the USB bulk transfer does not always guaranty the bandwidth, if the application has real time data transfer, e.g. data from data acquisition equipment, the FIFO master should consider to have extra buffer to handle the worst case data rate dip in the transfer.

2.2.5 FT601 data throughput demonstration

The demonstration is done with the FT600 Data Streamer application. The data rate below is a sustained and effective application data rate, measured when the transfer starts and the full data is collected at the other end.

The following figures are screen captures for the different FT601 configurations. The data is measured for the data transfer on a single channel as a time.

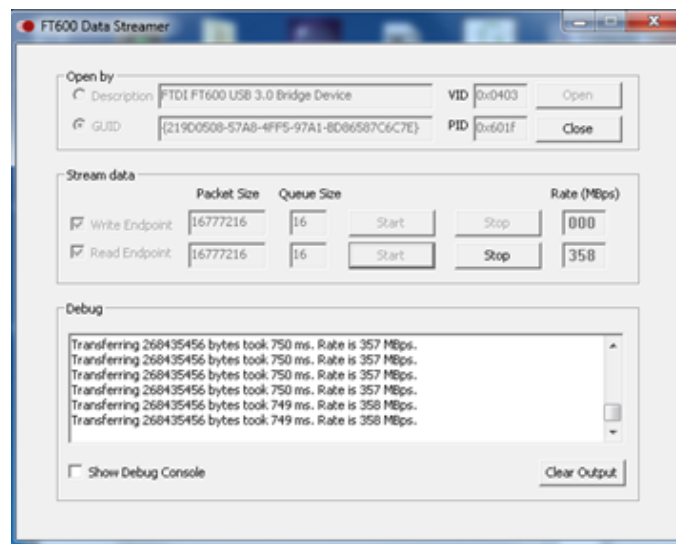


Figure 5 FT601 IN only

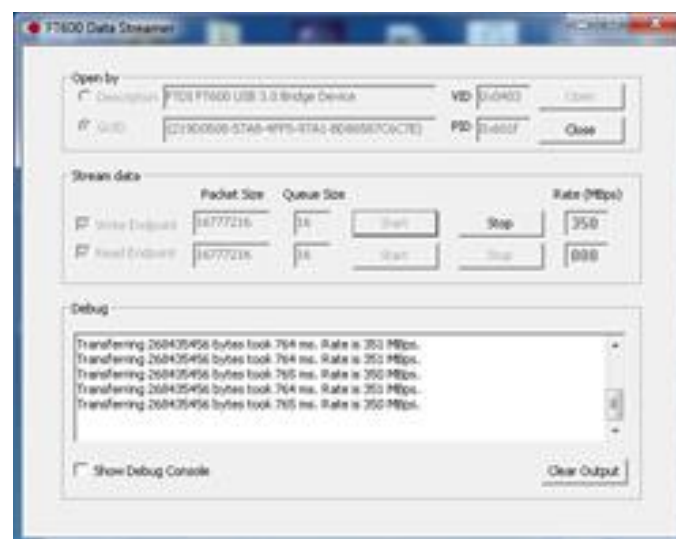


Figure 6 FT601 OUT only

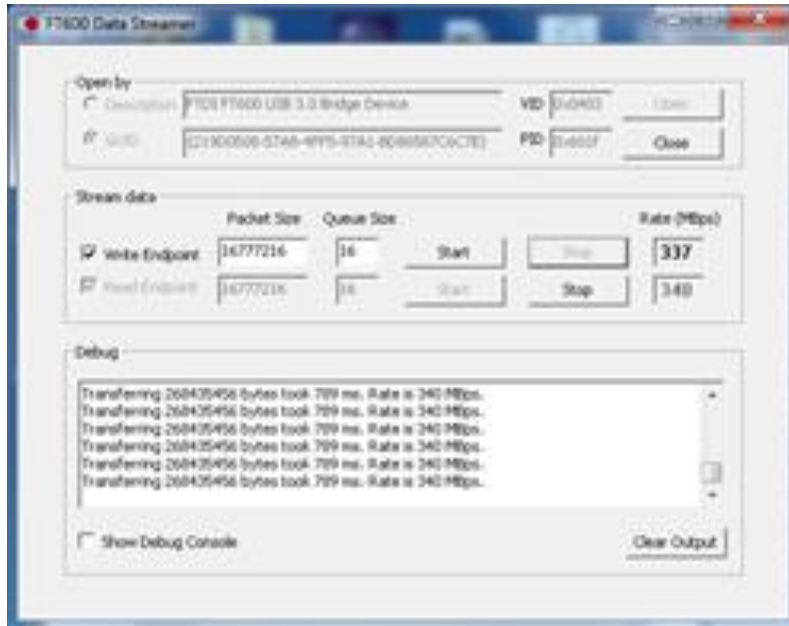


Figure 7 FT601 single Channel, IN transfer

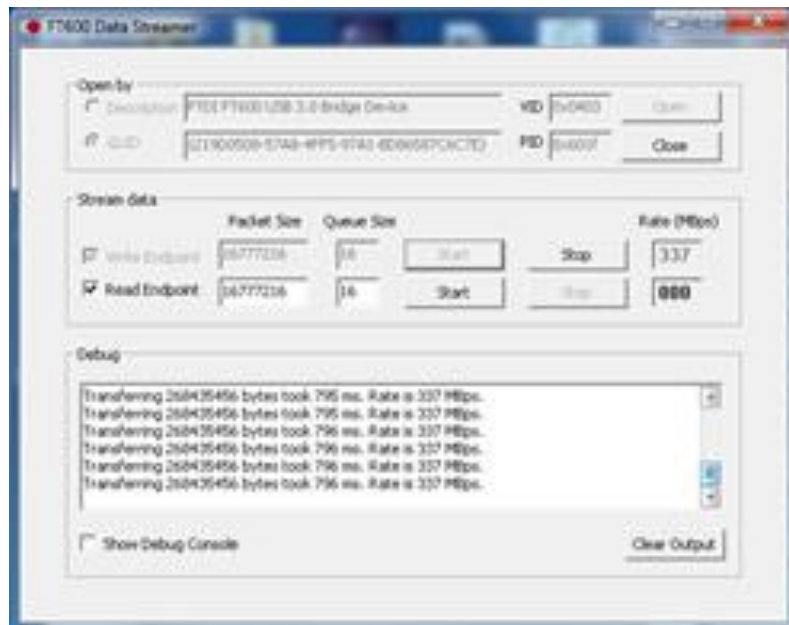


Figure 8 FT601 single Channel, OUT transfer

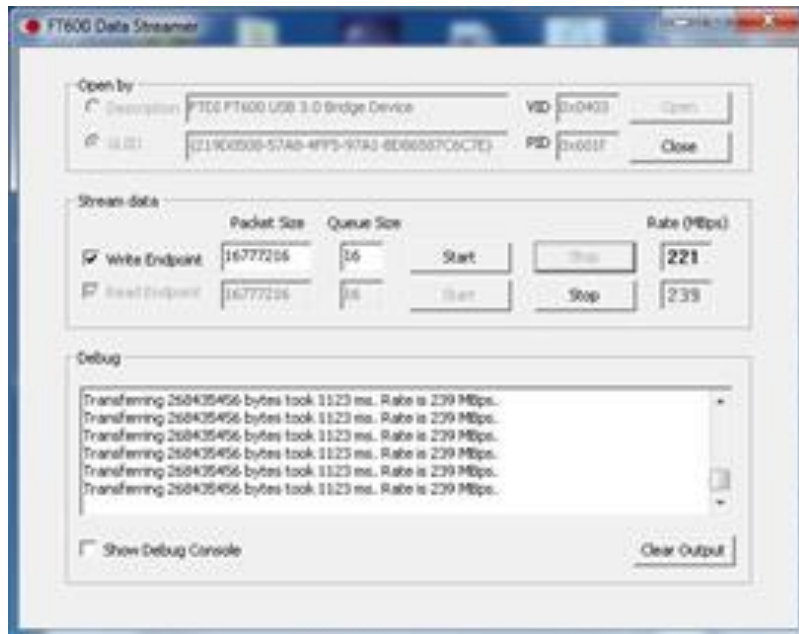


Figure 9 FT601 4 Channels, IN transfer

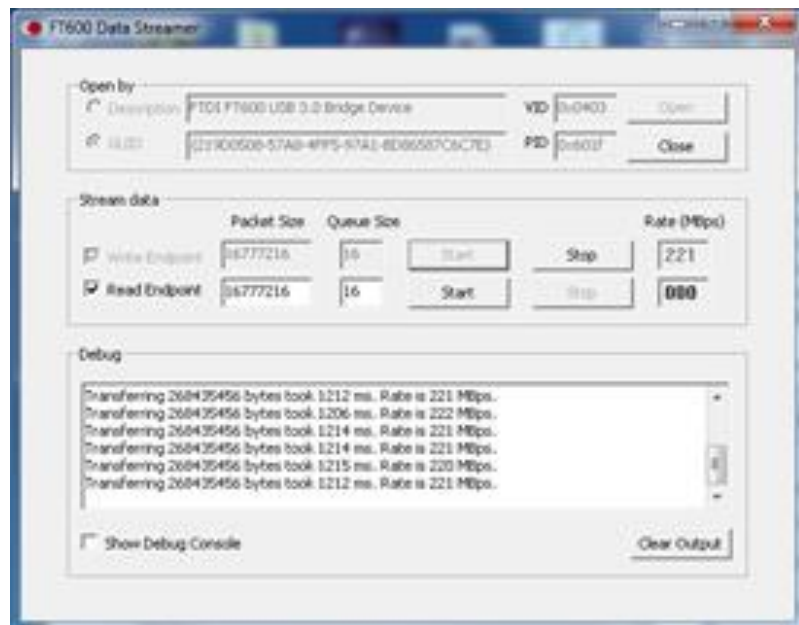


Figure 10 FT601 4 Channels, OUT transfer

3 Conclusion

The combination of several factors determines the best approach to reliable and optimized data flow for a given design. Some designs need a quick response while others require high data throughput. By using the details outlined in this application note, the optimal design can be achieved.

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Appendix A – References

Document References

[DS_FT600Q-FT601Q_IC_Datasheet](#)

[DS_UMFT60xx_Module_Datasheet](#)

[AN_370_FT600_Configuration_Programmer_User_Guide](#)

[AN_376_Xilinx_FPGA_FIFO_master_Programming_Guide](#)

[AN_379_D3XX_Programmers_Guide](#)

[AN_385_FTDI_D3XX_Driver_Installation_Guide](#)

Acronyms and Abbreviations

Terms	Description
API	Application Programming Interface
D3XX	FTDI Direct Device Driver & API for USB 3.0 bridge
USB	Universal Serial Bus
USB-IF	USB Implementers Forum

Appendix B – List of Tables & Figures

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Appendix C – Revision History

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